Patent

UNITED STATES PATENT APPLICATION

FOR

IMPROVING BARRIER FILM INTEGRITY ON POROUS LOW K DIELECTRICS BY APPLICATION OF A HYDROCARBON PLASMA TREATMENT

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Improving Barrier Film Integrity on Porous Low k Dielectrics by Application of a Hydrocarbon Plasma Treatment

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0001] The invention generally relates to the field of fabricating semiconductor devices. More specifically, it relates to the deposition of barrier films on porous dielectric material.

2. PRIOR ART

[0002] Modern integrated circuits generally contain several layers of interconnect structures fabricated above a substrate. The substrate may have active devices and/or conductors that are connected by the interconnect structure.

[0003] Current interconnect structures, typically comprising trenches and vias, are usually fabricated in, or on, an interlayer dielectric (ILD). It is generally accepted that, the dielectric material in each ILD should have a low dielectric constant (k) to obtain low capacitance between conductors. Decreasing this capacitance between conductors, by using a low dielectric constant (k), results in several advantages. For instance, it provides reduced RC delay, reduced power dissipation, and reduced cross-talk between the metal lines. For some cases, interconnect structures use dielectric materials such as silicon dioxide (SiO_2) or silicon oxyfluoride (SiOF). Articles discussing low k dielectrics are: "From tribological coatings to low-k dielectrics for ULSI interconnects," by A. Grill, Thin Solid Films 398-399 (2001) pages 527-532; "Integration Feasibility of Porous SiLK Semiconductor Dielectric," by J.J. Waterloos, et al., IEEE Conference Proceedings, IITC, (June 2001) pages 253-354; and "Low-k Dielectrics Characterization for Damascene

Integration, "by Simon Lin, et al., IEEE Conference Proceedings, IITC, (June 2001) pages 146-148.

[0004] However, dielectric materials may be extremely porous. The porous nature of dielectric material allows copper formed in the trenches and vias, without a barrier, to diffuse into an underlying layer causing the shorting of two adjacent copper lines or line-to-line leakage. Moreover, the surfaces of dielectric materials often possess openings or gaps where pores are exposed. Therefore, interconnect structures employ a barrier layer over the surface of the dielectric to protect from copper diffusing into the dielectric material. Common materials used for this barrier layer are Tantalum, Tantalum-Nitride, and Titanium Nitride.

[0005] Yet, any discontinuity, like discontinuities 130 in Figure 1a, in a thinly applied barrier film 120 will result in the diffusion of copper atoms or penetration of plating solution into a porous dielectric 110. This diffusion can also cause copper lines to short or leakage from line-to-line to occur. As shown in Figure 1b, prior art for highly porous dielectrics require the deposition of a thicker barrier layer 140, typically greater than 30nm, to physically cover the exposed pores to form a continuous barrier. Nevertheless, this thicker barrier layer takes up additional volume in a via or a trench increasing the resistance by reducing the volume available for copper.

BRIEF DESCRIPTION OF DRAWINGS

[0006] The embodiments of the present invention are illustrated by way of example and not in the figures of the accompanying drawings, in which references indicate similar elements and in which:

[0007] Figure 1a is a prior art cross-sectional elevation view of a trench and via defined by a porous interlayer dielectric, after a thin barrier layer has been deposited over the surface of the dielectric.

[0008] Figure 1b is a prior art cross-sectional elevation view of a trench and via defined by a porous interlayer dielectric, after a thick barrier layer has been deposited over the surface of the dielectric.

[0009] Figure 2 is a cross-sectional elevation view of a trench and via defined by a porous dielectric material that is disposed above an etch stop/diffusion barrier formed on an underlying layer.

[0010] Figure 3 illustrates the structure of Figure 2 after the surface of the porous dielectric has been treated.

[0011] Figure 4 illustrates the structure of Figure 3 after a barrier layer is deposited over the treated surface of the interlayer dielectric, so as to line the via and the trench.

[0012] Figure 5 illustrates the structure of Figure 4 after copper alloy is formed over the barrier layer, so as to fill the via and the trench.

[0013] Figure 6 illustrates the structure of Figure 5 after the copper alloy is planarized.

[0014] Figure 7 illustrates the Delta and Psi angles when toluene is used as a probe solvent on 20nm of Ta deposited over untreated Zirkon 2000 as compared to Zirkon 2000 treated by a high power C_2H_4 plasma and a low power C_2H_4 plasma.

DETAILED DESCRIPTION

[0015] A method for improving barrier film integrity on porous dielectrics by application of hydrocarbon plasma treatment is described. In the following description, numerous specific details are set forth, such as specific materials and thicknesses in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps, such as masking and etching steps, have not been described in detail in order to avoid unnecessarily obscuring the present invention.

[0016] Referring first to Figure 2, an underlying layer 205 is illustrated, which often is comprised of several active devices and/or a layer with metal exposed. Underlying layer 205 may be a semiconductor wafer including device regions, other structures such as gates, local interconnects, metal layers, or other active/passive device structures or layers. An etch stop/diffusion barrier 210 is also illustrated in Figure 2, which can be comprised of numerous materials. For example, etch stop/diffusion barrier 210 may be comprised of silicon nitride (Si_3N_4) or silicon carbide (SiC).

[0017] Figure 2 further illustrates a porous interlayer dielectric (ILD), such as ILD 215, which is deposited on etch stop/diffusion barrier 210. ILD 215 may be formed from any one of a plurality of known dielectric materials. In one embodiment of the present invention, ILD 215 is formed from a low k dielectric such as a polymer-based dielectric. In another embodiment, a non-organic material such as a carbon-doped oxide with induced porosity is used. In yet another embodiment, Zirkon 2000 is used as the

dielectric material. Zirkon 2000 may be spun-coated onto etch stop/diffusion barrier 210, an underlying layer, or a silicon wafer.

[0018] One category of low k materials, the organic polymers, are typically spun-on. A discussion of perfluorocyclobutane (PFCB) organic polymers is found in, "Integration of Perfluorocyclobutane (PFCB)." By C.B. Case, C.J. Case, A. Kornblit, M. E. Mills, D. Castillo, R. Liu, Conference Proceedings, ULSI XII.CPOYRGT. 1997, Materials Research Society, beginning at page 449. These polymers are available from companies such as Dupont, Allied Signal, Dow Chemical, Dow Corning, and others.

[0019] Another category of low k materials that may be used in the present invention are silica-based such as the nanopouous silica aerogel and xerogel. These dielectrics are discussed in "Nanoporous Silica for Dielectric Constant Less than 2," by Ramos, Roderick, Maskara and Smith, Conference Proceedings ULSI XII.COPYRGT. 1997, Materials Research Society, beginning at page 455 and "Porous Xerogel Films as Ultra-Low Permittivity Dielectrics for ULSI Interconnect Applications," by Jin, List, Lee, Lee, Luttmer and Havermann, Conference Proceedings ULSI XII.COPYRGT. 1997, Materials Research Society, beginning at page 463.

[0020] After forming ILD 215, vias and trenches, such as via 220 and trench 225 in Figure 2, are etched into ILD 215 and through etch stop/diffusion barrier 210. Ordinary masking and etching processes are used to form trench 220, via 225, and any other trenches or vias needed within ILD 215.

[0021] Next the surface of ILD 215 is treated with hydrocarbon plasma, so as to deposit a thin coating of carbon-rich polymeric material, such as carbon-rich polymer layer 310 in Figure 3, on the surface of the low k dielectric. The plasma approach allows

the deposition of a uniform thin polymer inside small structures, such as via 220 and trench 225, used in advance microelectronic interconnect fabrication.

[0022] Hydrocarbon plasma is generated using a hydrocarbon source gas in a plasma chamber. In one embodiment, C_2H_4 may be used as the hydrocarbon gas source. In another embodiment, other gas sources may be used including C_3H_6, CH_4, and other hydrocarbons. Numerous common plasma chambers, from suppliers such as AMAT and Lam, may be used for generating the hydrocarbon plasma. The plasma may be generated over a wider range of variable pressure, power, bias, and time. The following ranges are a non-limitave illustration of the ranges for C_2H_4 plasma generation: pressure of 7-60 mTorr, power for 500W to 1700W, bias of 0 to 300W, and for a time 3-10 seconds. As an illustrative example, a C_2H_4 plasma may be generated in a Lam 9100 etch chamber at approximately 7mTorr of pressure, 500 Watts of power, and 0 Watts of bias exposing the dielectric to this plasma for approximately 10 seconds. As another illustrative example, a C_2H_4 plasma may be generated in a Lam 9100 etch chamber at approximately 7mTorr of pressure, 1700 Watts of power, and 300 Watts of bias exposing the dielectric to this plasma for approximately 10 seconds.

[0023] As Figure 4 illustrates, a blanket barrier layer 410, is formed on the treated surface of ILD 215. The barrier material may react with the carbon-rich polymer surface during deposition to form an interfacial carbide layer 405 and may catalyze cross-linking of carbon. In one embodiment, the barrier material is comprised of tantalum (Ta). In another embodiment, the barrier material is comprised of tantalum nitride (TaN). Other materials, such as Ta/TaN bilayers, TiN, WCN, TiSiN, may be used as the barrier material. Tantalum may be deposited using known methods of deposition, such as

physical vapor deposition (PVD). Other methods of deposition may include ALD (atomic layer deposition) and MOCVD (metalorganic chemical vapor deposition).

[0024] The carbon-rich polymer allows a thinner film of barrier material to be deposited to form a continuous sealed barrier. Even though, the barrier film is thinner than prior art requires, it is a more robust barrier than possible without hydrocarbon plasma treatment. Therefore, one may deposit less than prior art ranges of 30nm or more of barrier material and receive more protection from penetration. As an illustrative example, experimental evidence shows that 20nm of tantalum deposited on C_2H_4 plasma-treated Zirkon 2000 dielectric, within the aforementioned ranges in generating hydrocarbon plasma, seals the dielectric to toluene vapor. Yet, 20nm of tantalum on untreated Zirkon 2000 does not seal the Zirkon 2000 to toluene vapor. Furthermore, prior art would require more than 30nm of tantalum to provide a barrier sufficient to block penetration of toluene.

[0025] The following experiment was conducted to experimentally verify the aforementioned illustrative example. Zirkon 2000 was spun-coated onto a 200mm silicon wafer and cured. Blanket films were then exposed to the hydrocarbon plasma treatment. A C_2H_4 plasma was generated in a Lam 9100 etch chamber at approximately 7mTorr and was exposed to the Zirkon 2000 for 10 seconds. Two different power and bias voltages were applied (C_2H_4 high W: 1700W power and 300W bias and C_2H_4 low W: 500W power and 0W bias). 20nm of Tantalum was deposited by PVD in an AMAT Electra SIP chamber on untreated Zirkon 2000 and on Zirkon 2000 exposed to the C_2H_4 high W and the C_2H_4 low W plasmas. Wafers were then measured for porosity in an XPEQT EP-10 ellisometric porosimetry tool with toluene as the probe solvent. Figure 7 shows the

optical response of the films to the introduction of toluene in a vacuum. Films that allow the penetration and absorption of toluene inside the pore structure will change the optical properties of the film. As Figure 7 illustrates from curve 750, the untreated Zirkon 2000's optical values Psi (axis 710) and Delta (axis 720) change during the introduction of toluene. In contrast, the two treated films (C_2H_4 high W as shown by curve 740 and the C_2H_4 low W as shown by curve 730) do not show change in optical properties indicating a sealed barrier film to toluene.

[0026] Next, an ordinary plating process is used to form the copper or copper alloy layer 510, as shown in Figure 5.

[0027] As shown in Figure 6, the structure of Figure 5 is now planarized, removing copper alloy layer 510, barrier layer 410, and interfacial carbide layer 405 from the upper surface of the dielectric.

[0028] As an illustrative example, planarizing can be done by either chemical-mechanical polish (CMP) or electropolishing. Both CMP and electropolishing techniques for planarizing are well known. Electropolishing and related technology is described in U.S. Patents 5,096,550; 6,017,437; 6,143,155; and 6,328,872.

[0029] Furthermore, these methods described above may be repeated to create multilayered interconnect structures.

[0030] Thus, as explained above using hydrocarbon plasma treatment on the surface of porous dielectrics, allows one to use thinner barrier layers to protect from diffusion and penetration of copper atoms and plating solution. Therefore, a thinner barrier layer takes up less volume in a via or a trench decreasing the resistance by increasing the volume available for copper. The foregoing description has been in reference to specific

embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. Therefore, the scope of the invention should be limited only by the appended claims.